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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,254	02/23/2004	Linyong Pang	NTI-849	8873

29477 7590 11/14/2005

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,254	PANG, LINYONG	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/23/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/785,254 filed on 02/23/2004. Claims 1 – 21 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 8, before "characterizing" insert —**the**—.
Claim 4, line 8, before "characterizing" insert —**the**—.
Claim 12, line 8, before "characterizing" insert —**the**—.
Claim 4, line 8, before "characterizing" insert —**the**—.
Claim 10, line 2, rephrase —**resist information**—.
Claim 11, line 2, rephrase —**resist information**—.
Claim 15, line 8, before "feature" insert —**the**—.
Claim 15, line 9, before "wafer" insert —**accurate**—.
Claim 15, line 9, after "locations" insert —**of the feature**—.
Claim 15, line 10, after "information" insert —**of the feature**—.
Claim 15, line 12, before "matching" insert —**the**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1 – 21 are rejected under 35 U.S.C. 102(a) as being unpatentable over U.S. Patent No. 6,577,994 B1 to *Tsukuda*.

5. As to Claim 15, *Tsukuda* shows and discloses the following subject matter:

- A method of setting a *threshold value* of a photomask feature...a *threshold value* is determined based on an *exposure energy* and *sensitivity of a resist* – [col. 9, line 33 – col. 10, line 29]; Notice that data of threshold value is evaluated and determined based on results obtained of a *test layout*, which is to be formed on resist on a wafer;
- Dimension (finished size) of a pattern formed on a resist (on a wafer) is predicted based on the result of *optical simulation* (i.e., *wafer simulation*) – [abstract];
- Simulating a feature (on a test layout) using a *resist model*, which taking into account of *resist effect* and *etching effect* etc. into account, thereby providing accurate contour (i.e., accurate feature edge locations, finished size) of feature in the test layout formed on the resist on a wafer – [col. 14, line 11 – 19; Fig. 8]; Simulating the feature on the test layout using an optical model, which provides aerial image information (finished size) of the (finished) feature in the test layout formed on the wafer without taking consideration of *resist effect* and *etching effect* – [col. 10, line 1 – 14; Fig. 8]
- Comparing the accurate feature contour (finished size) to the aerial image information of the finished size of the feature under study formed on the wafer – [col. 9, line 66 – col. 10, line 29; Fig. 8]; Notice that the threshold (i.e., difference in light intensity – exposure margin) in exposure energy of the feature under study is computed by matching the accurate feature contour to the aerial image information of the finished size of the feature formed on the wafer;
- Storing the threshold in a *look-up table* (LUT) – [Fig. 20].

Notice that (1) the method listed above is applied to generate thresholds for a plurality of features on the test layout (2) the thresholds are organized and stored in the look-up table for design reference.

For reference purposes, the explanations given above in response to Claim 15 are called **[Response A]** hereinafter.

6. As to Claim 1, *Tsukuda* shows and discloses the following subject matter:

- A method of automatically performing a *optical simulation* (i.e., *wafer simulation*) – [abstract; Fig. 1; Fig.17];
- *Resist patterns* formed wafers ... mask patterns for forming the resist patterns – [col. 1, line 14 – 23]; Optical simulation *mask pattern* is a *mask image*, which is design based on a circuit pattern;
- Performing *optical simulation* (*wafer simulation*) of a mask pattern for predicting the *shape of a finished (resist) pattern* on a wafer – [col. 1, line 49 – 65]; Notice that the *optical simulation* is performed base on an *optical model*;
- Optical simulation is performed to *characterize* sizes (i.e., line width, space width, pattern) of a *feature* (e.g., line) of a mask pattern in predicting *finished size/contour of feature (line)* of an associated circuit pattern to be formed on a *resist on a wafer* – [abstract; col. 9, line 66 – col. 10, line 29; Fig. 17];
- Obtaining a *threshold value (data)* of *exposure energy* employing a *resist model*, which take into consideration of *resist effect* and/or *etching effect* related to resolvability of size and pattern of a feature under study – [col. 14, line 2 – 19]; Threshold value of exposure (energy) value is associated with finished sizes (i.e., line width, space width, pattern) of a feature under study– [col. 10, line 1 – 29]; Therefore, a threshold value is associated to a feature to be finished on a resist using a specified exposure energy;
- Applying a threshold value to an optical simulation to generate accurate feature contours on a resist on a wafer – [abstract; col. 10, line 1 – 29].
- A set of *data of threshold value* provided for use in *optical simulation* (*wafer simulation*) is stored in a look-up table for design reference – **[Response A**; Fig. 20].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response B]** hereinafter.

7. As to Claim 12, reasons are included in **[Response B]** given above.

8. As to Claim 4, reasons are included in **[Response B]** in given above. Notice that a threshold value which is generated based on one resist model (e.g., first model) taking into account of both resist effect and etching effect is more accurate than a threshold

value which is generated based on another resist model (e.g., second model) taking into account only resist effect.

9. As to Claim 7, reasons are included in **[Response B]** in given above. *Tsukuda* shows in Fig. 17 and discloses that *resist information* includes *light intensity data* (I.e., *optical information*) and information regarding *resist effect* and *etching effect* – [Fig. 17; col. 14, line 1 – 19].

For reference purposes, the explanations given above in response to Claim 7 are called **[Response C]** hereinafter.

10. As to Claims 10 and 11, reasons are included in **[Response C]** given above.

11. As to Claim 8, a resist pattern contour contains many features of different sizes (line width, pitch size) and shape. Therefore, in a photomask for generating the resist pattern contour on a wafer contains many mask features, and each mask feature has an associated threshold. Information of mask features and associated thresholds can be accessed from the LUT as shown in Fig. 20.

For reference purposes, the explanations given above in response to Claim 8 are called **[Response D]** hereinafter.

12. As to Claim 21, reasons are included in **[Response D]** given above.

13. As to Claims 2, 5, 9, 13, 16 and 17, reasons are included in **[Response B]** given above. Notice that threshold value is a function of *line width* (i.e., *feature size*), space width (i.e., *patch size*) and *pattern shape* associated with a mask feature. *Tsukuda* disclose various thresh values ... a plurality of finished sizes – [col. 10, line 25 – 29]; Therefore, it is anticipated that, for easy retrieval, the threshold data in the LUT is organized based on feature size, pitch size and patter shape as illustrated in Fig. 20.

14. As to Claims 3, 6 and 14, *Tsukuda* shows and discloses the subject matter in – [Fig. 17; col. 10, line 14 – 45]. *Tsukuda* also teaches that it is possible to in *precision* of a consideration of an exposure margin by increasing the number of threshold values –

[col. 10, line 42 – 45]. Therefore, it is anticipated that one threshold value may achieve a closest match; whereas another threshold value may achieve an exact match. Notice that, information regarding threshold data which is an exact match or a closely match can be obtained; it should be stored in the LUT for design reference or future retrieval.

15. As to Claim 18, each resist has its own optical sensitivity; threshold of a feature is a function of the optical sensitivity. For a given feature, different resist requires different threshold. Taking into consideration of various resist optical sensitivity, LUT can include thresholds for more than one resist.

16. As to Claim 19, *Tsukuda* shows and discloses the subject matter in – [Fig. 8 – Fig. 11].

17. As to Claim 20, since threshold value is a function of *line width* (*feature size*), space width (*patch size*) and *pattern shape*, to general a complete and useful set of thresholds in the LUT, the test layout should include various patterns, pitch sizes, and feature sizes.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
November 10, 2005